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APR 23 2007

REMARKS

Claims 10-12 and 25-31 are pending. Claims 10, 25, and 27-31 are rejected under 35 U.S.C. § 102(b). Claims 10 and 12 are currently amended.

Claim 12 is objected to for reciting "producing less than the plurality of channel estimates." Applicants have amended claim 12 to recite "producing at least one channel estimate less than the plurality of channel estimates in response to the other of the first control signal and the second control signal." This is explained in detail with reference to Figure 7A at pages 10-11 of the instant specification. Therein, when the output signal λ is greater than η_1 , the comparator circuit produces a control signal on lead 728 indicating no transmit diversity, and channel estimate α_j^2 is set to zero. Only channel estimate α_j^1 is produced. (page 10, lines 14-18). Alternatively, when the output signal λ is less than η_2 , the comparator circuit produces a control signal on lead 728 indicating transmit diversity, and the WMSA circuit 732 produces both channel estimates α_j^1 and α_j^2 . (page 10, line 25 through page 11, line 3).

Claim 10 is rejected under 35 U.S.C. § 102(b) as being anticipated by either applicants' admitted prior art (AAPA) or Feldman (U.S. Pat. No. 4,983,981). Claim 10 is amended to recite "producing a first control signal **indicating one of transmit diversity and no transmit diversity of the input signal** in response to the step of comparing when the output signal has a value greater than a value of the first reference signal; comparing the output signal to a second reference signal; and producing a second control signal **indicating the other of transmit diversity and no transmit diversity of the input signal** in response to the step of comparing when the output signal has a value greater than a value of the second reference signal." (emphasis added). Applicants believe this clearly distinguishes over either AAPA or Feldman. Thus, claim 10 is patentable under 35 U.S.C. § 102(b).

Claims 25-31 are rejected under 35 U.S.C. § 102(b) as being anticipated by applicants' admitted prior art (AAPA). As best applicants understand the present rejection, Examiner now

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relies on the WMSA circuit of Figure 5 as disclosing elements of claims 25 and 29. Applicants respectfully disagree for the following reasons. The WMSA circuit of the prior art comprises only part of the WMSA block 732 of the present invention. For example, two WMSA circuits (Figure 5) are included in WMSA block 732. One produces channel estimate α_j^1 at lead 734, and the other produces α_j^2 at lead 736. Neither receives a control signal corresponding to a number of transmit antennas as recited in claims 25 and 29. The control signal is produced by comparator circuit 726 (Figure 7A) as explained at page 10, lines 12-23 of the instant specification. Examiner will note that lead 728 (Figure 7A) is not applied directly to the WMSA circuit of Figure 5. Furthermore, the WMSA circuit of Figure 5 does not include a correction circuit or a decoder circuit as recited in claim 25. Moreover, the WMSA circuit of Figure 5 does not selectively combine the input signal in response to the control signal or decode the input signal as recited by claim 29. Thus, applicants respectfully submit that claims 25-31 are patentable under 35 U.S.C. § 102(b) over AAPA.

In view of the foregoing, applicants respectfully request reconsideration and allowance of claims 10-12 and 25-31. If Examiner finds any issue that is unresolved, please call applicants' attorney by dialing the telephone number printed below.

Respectfully submitted,



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